REMARKS

This responds to the Final Office Action mailed on May 30, 2008.

Claims 7, 22 and 29 are amended, no claims are canceled, and no claims are added; as a result, claims 7, 8, 14, 15, 22, 24, 25 and 29-32 remain pending in this application.

§112 Rejection of the Claims

Claims 31 and 32 were rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate description or enablement.

Applicant respectfully submits that the specification, for example, p. 17, line 21 through p. 18, line 8, describes the subject matter claimed in claims 31 and 32 in such a way to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. For example, the cited portion of the specification describes that "the FOQ is logically two separate queues...: one queue for accesses to the Dcache, and one queue for accesses to the Ecache. ... An FOQ entry that is marked to access both the Ecache and Dcache may logically be dequeued from the Ecache queue before being dequeued from the Dcache queue. After doing so, the request will still remain in the FOQ, but be marked only as a Dcache request ... for a write request which is able to send its write through to the Ecache, but not yet able to write to the Dcache." It is inherent that the Dcache queue and the Ecache queue check (i.e., monitor) the status of a corresponding memory request to mark it as an Ecache request and/or Dcache request.

Claims 29-32 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Claim 29 has been amended to more clearly define Applicant's claimed invention. Claims 30 and 31 are dependent on claim 29 and, therefore, more clearly define Applicant's claimed invention based on the amendment to claim 29. Claim 32 is dependent on claim 22 and is definite based on its relationship to claim 22.

§103 Rejection of the Claims

Claims 7, 8, 22, 24, 25 and 29-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes (US 6,393,5356) in view of Henry et al. (US 2003/0018875)and in

further view of Hennessy et al. (*Computer Organization and Design: The Hardware / Software Interface*). Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes in view of Henry et al. and in further view of Hennessy et al. as applied to claim 7 , and in further view of Yamahata (US 5,2479,639).

Applicant respectfully submits that none of the cited documents, alone or in combination, teach or suggest features taught by Applicant and claimed in claims 7, 22 and 29, as amended.

Under Hughes' approach, all memory operations are moved from LS1 buffer 60 to LS2 buffer 62 once data cache 28 is initially probed. The move from LS1 buffer 60 to LS2 buffer is made independent of the result of the probe status (e.g., whether the operation hits or misses in data cache 28). See e.g., id. at col. 14, lines 20-34 and col. 16, lines 61-66. If the memory operation is a store operation, it is held in the LS2 buffer until the memory operation can be committed. See id. at col. 16, lines 61-66. If the memory operation is a load operation, it is checked to determine whether the "load hits a store" in the LS2 buffer. See id. at col. 26, lines 6-31, Fig. 3 ("hit/miss" signal 82) and Fig. 6 (a flowchart illustrating the operation of the LS2 control logic). If the load does not "hit a store" in the LS2 buffer, then the LS2 logic associated with the LS2 buffer determines if the load operation is a hit in the data cache 28. See id. That is, under Hughes' approach, two conditions are checked after the memory operations are moved to, and held in LS2: 1) whether an incoming memory request's address matches that of an existing memory request and 2) whether the incoming memory request hits in the data cache 28.

In contrast, under Applicant's approach, the local cache is checked while the incoming memory request is held in an Initial Request Queue (IRQ) (i.e., before the memory request is moved, if ever, to a Forced Order Queue (FOQ)). Likewise, a check is made to determine whether a portion of an address associated with the incoming memory request matches one or more partial addresses existing in the FOQ before the memory request is moved, if ever, to the FOQ. As described by Applicant and claimed in claims 7, 8, 14, 15, 22, 24, 25, and 29-32, "if the portion of an address associated with the memory request does not match the one or more partial addresses in the FOQ and, at the same time, the memory request misses in the local cache" the memory request is added to the FOQ.

That is, in contrast to Hughes, the determination of whether a memory request is to be added to the FOQ is conditioned on "if the portion of an address associated with the memory

request does not match the one or more partial addresses in the FOQ" and, at the same time, whether "the memory request misses in the local cache". Claims 7, 22 and 29 have been amended to underscore this distinction.

Claims 8, 14, 15, 24, 25 and 30-32 are allowable as being dependent on one of corresponding independent claims 7, 22 and 29 which are believed to be allowable.

Reconsideration and allowance of claims 7, 8, 14, 15, 22, 24, 25, and 29-32 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

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By Thomas F. Brennan
Thomas F. Brennan
Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 30, 2008.

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Name

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